ACT334

Rev 2, 14-Nov-12

High Performance *ActivePSR™* Primary Switching Regulator

FEATURES

- **Ultra Low Standby Power < 30mW**
- **Patented Primary Side Regulation Technology**
- **Suitable Operation Frequency up to 85kHZ**
- **Proprietary Fast Startup Circuit**
- **Integrated Line and Primary Inductance Compensation**
- **Integrated Programmable Output Cord Resistance Compensation**
- **Line Under-Voltage, Output Over-Voltage, Output Short-Circuit and Over-Temperature Protection**
- **Complies with all Global Energy Efficiency and CEC Average Efficiency Standards**
- **Adjustable Power from 2W to 6W**
- **Minimum External Components**
- **Tiny SOT23-6 Package**

APPLICATIONS

- **Chargers for Cell Phones, PDAs, MP3, Portable Media Players, DSCs, and Other Portable Devices and Appliances**
- **RCC Adapter Replacements**
- **Linear Adapter Replacements**
- **Standby and Auxiliary Supplies**

GENERAL DESCRIPTION

The ACT334 belongs to the high performance patented *ActivePSR™* Family of Universal-input AC/DC off-line controllers for battery charger and adapter applications. It is designed for flyback topology working in discontinuous conduction mode (DCM). The ACT334 meets all of the global energy efficiency regulations (CEC, European Blue Angel, and US Energy Star standards) while using very few external components.

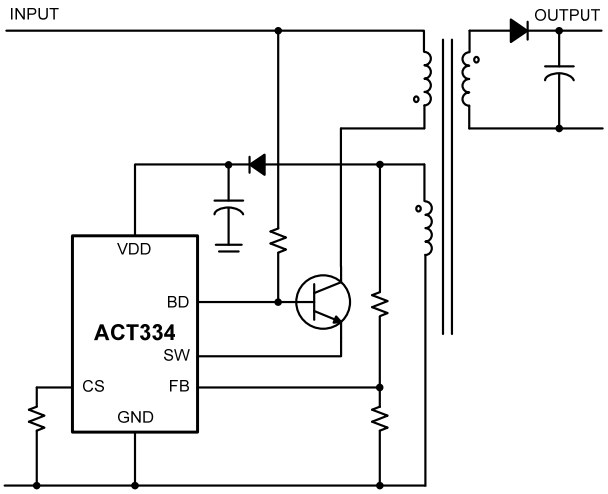
The ACT334 ensures safe operation with complete protection against all fault conditions. Built-in protection circuitry is provided for output short-circuit, output over-voltage, line under-voltage, and over temperature conditions.

The ACT334 *ActivePSR™* is optimized for high performance, cost-sensitive applications, and utilizes Active-Semi's proprietary primary-side feedback architecture to provide accurate constant voltage, constant current (CV/CC) regulation without the need of an opto-coupler or reference device. Integrated line and primary inductance compensation circuitry provides accurate constant current operation despite wide variations in line voltage and primary inductance. Integrated output cord resistance compensation further enhances output accuracy. The ACT334 achieves excellent regulation and transient response, yet requires less than 30mW of standby power.

The ACT334 is optimized for compact size 2W to 6W charger applications. It is available in space-saving 6 pin SOT23-6 package.

Figure 1:

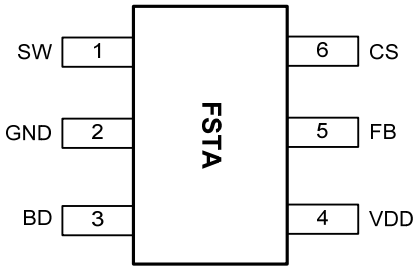
Simplified Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT334US-T	-40°C to 85°C	SOT23-6	6	TAPE & REEL	FSTA

PIN CONFIGURATION



SOT23-6
ACT334US-T

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	SW	Switch Drive. Switch node for the external NPN transistor. Connect this pin to the external power NPN's emitter. This pin also supplies current to VDD during startup.
2	GND	Ground.
3	BD	Base Drive. Base driver for the external NPN transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	FB	Feedback Pin. Connect this pin to a resistor divider network from the auxiliary winding.
6	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch. The peak current limit is set by (0.396V × 0.9) / R_{CS}. For more detailed information, see Application Information.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VDD, BD, SW to GND	-0.3 to + 28	V
Maximum Continuous VDD Current	100	mA
FB, CS to GND	-0.3 to + 6	V
Continuous SW Current	Internally limited	A
Maximum Power Dissipation (derate 4.5mW/˚C above T_A = 50˚C)(SOT23-6)	0.45	W
Junction to Ambient Thermal Resistance (θ_{JA})(SOT23-6)	220	˚C/W
Operating Junction Temperature	-40 to 150	˚C
Storage Junction	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 14V, V_{OUT} = 5V, L_P = 1.6mH, N_P = 140, N_S = 8, N_A = 23, T_A = 25°C, unless otherwise specified.)

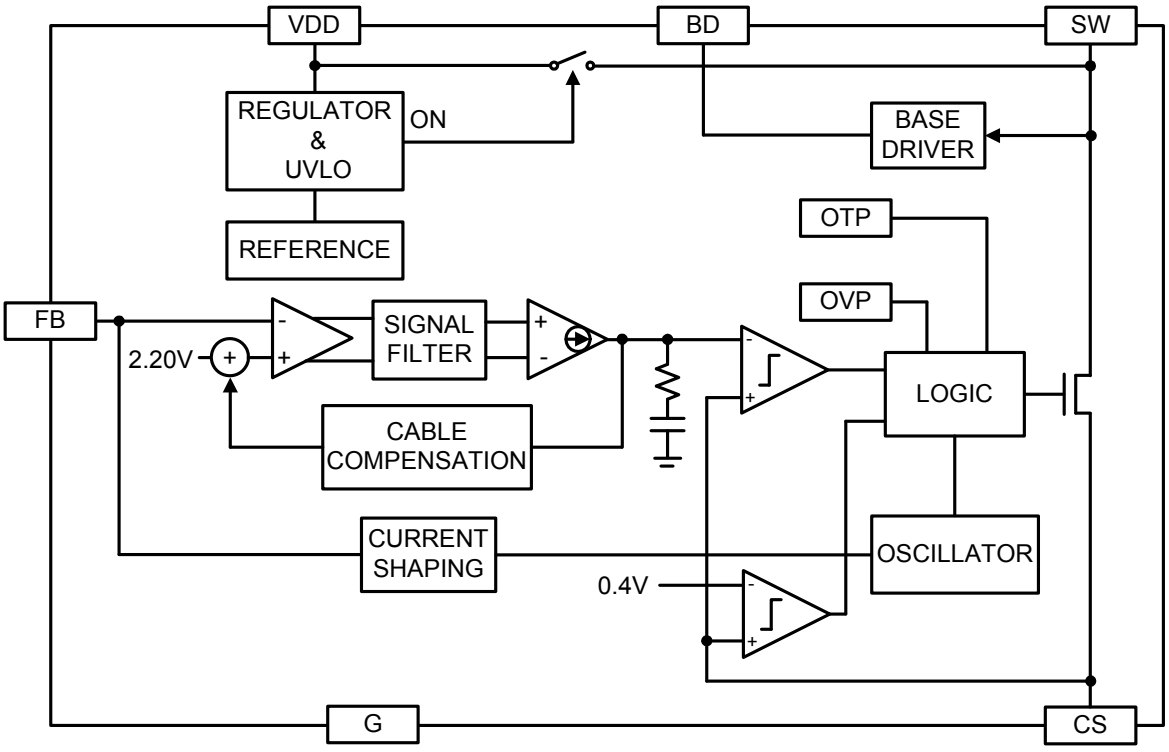
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	17.6	18.6	19.6	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	5.25	5.5	5.75	V
Supply Current	I_{DD}	V_{DD} = 14V, after Turn-on	240	340	440	uA
Start Up Supply Current	I_{DDST}	V_{DD} = 14V, before Turn-on		25	45	μA
BD Current during Startup	I_{BDST}				1	μA
Internal Soft Startup Time				10		ms
Oscillator						
Switching Frequency	f_{SW}	100% V_{OUTCV} @ full load		80		kHz
		25% V_{OUTCV} @ full load		40		
Maximum Switching Frequency	F_{CLAMP}		89	98	107	kHz
Maximum Duty Cycle	D_{MAX}		65	75	85	%
Feedback						
Effective FB Voltage	V_{FB}		2.17	2.192	2.216	V
FB Leakage Current	I_{FBLK}				1	μA
Output Cable Resistance Compensation	DV_{COMP}	No R_{CORD} between VDD and SW		0		%
		R_{CORD} = 300k		3		
		R_{CORD} = 150k		6		
		R_{CORD} = 75k		9		
		R_{CORD} = 33k		12		

ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = 14V, V_{OUT} = 5V, L_P = 1.5mH, N_P = 140, N_S = 8, N_A = 23, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
SW Current Limit Range	I_{LIM}		100		600	mA
CS Current Limit Threshold	V_{CSLIM}	t_{OFF_DELAY} = 0	380	396	412	mV
Leading Edge Blanking Time			200	300		ns
Driver Outputs						
Switch ON-Resistance	R_{ON}	I_{SW} = 50mA		1.6	3	Ω
SW Off Leakage Current		V_{SW} = V_{DD} = 22V			1	μA
Protection						
VDD Latch-Off Voltage	V_{DDOVP}		V_{DDON} +2	V_{DDON} +3	V_{DDON} +4	V
Thermal Shutdown Temperature				135		˚C
Thermal Hysteresis				20		˚C
Line UVLO	I_{FBUVLO}			134		μA

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the *Functional Block Diagram,* to regulate the output voltage in CV (constant voltage) mode, the ACT334 compares the feedback voltage at FB pin to the internal reference and generates an error signal to the pre-amplifier. The error signal, after filtering out the switching transients and compensated with the internal compensation network, modulates the external NPN transistor peak current at CS pin with current mode PFWM (Pulse Frequency and Width Modulation) control. To regulate the output current in CC (constant current) mode, the oscillator frequency is modulated by the output voltage.

SW is a driver output that drives the emitter of an external high voltage NPN transistor. This base-emitter-drive method makes the drive circuit the most efficient.

Fast Startup

VDD is the power supply terminal for the ACT334. During startup, the ACT334 typically draws only 25μA supply current. The startup resistor from the rectified high voltage DC rail supplies current to the base of the NPN transistor. This results in an amplified emitter current to VDD through the SW pin via Active-Semi's proprietary fast-startup circuitry until it exceeds the V_{DDON} threshold 19V. At this point, the ACT334 enters internal startup mode with the peak current limit ramping up in 10ms. After switching starts, the output voltage begins to rise. The VDD bypass capacitor must supply the ACT334 internal circuitry and the NPN base drive until the output voltage is high enough to sustain VDD through the auxiliary winding. The V_{DDOFF} threshold is 5.5V; therefore, the voltage on the VDD capacitor must remain above 5.5V while the output is charging up.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT334 captures the auxiliary flyback signal at FB pin through a resistor divider network R5 and R6 in Figure 6. The signal at FB pin is pre-amplified against the internal reference voltage, and the secondary side output voltage is extracted based on Active-Semi's proprietary filter architecture.

This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 2.20V \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \times \frac{N_S}{N_A} - V_D \qquad (1)$$

where R_{FB1} (R5) and R_{FB2} (R6) are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_D is the rectifier diode forward drop voltage at approximately 0.1A bias.

Standby (No Load) Mode

In no load standby mode, the ACT334 oscillator frequency is further reduced to a minimum frequency while the current pulse is reduced to a minimum level to minimize standby power. The actual minimum switching frequency is programmable with an output preload resistor.

Loop Compensation

The ACT334 integrates loop compensation circuitry for simplified application design, optimized transient response, and minimal external components.

Output Cable Resistance Compensation

The ACT334 provides programmable output cable resistance compensation during constant voltage regulation, monotonically adding an output voltage correction up to predetermined percentage at full power. There are four levels to program the output cable compensation by connecting a resistor (R10 in Figure 6) from the SW pin to VDD pin. The percentage at full power is programmable to be 3%, 6%, 9% or 12%, and by using a resistor value of 300k, 150k, 75k or 33k respectively. If there is no resistor connection, there is no cord compensation.

This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cable resistance.

Constant Current (CC) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT334 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting

FUNCTIONAL DESCRIPTION CONT'D

in a constant secondary side output current profile. The energy transferred to the output during each switching cycle is ½(L_P × I_{LIM}^2) × η, where L_P is the transformer primary inductance, I_{LIM} is the primary peak current, and η is the conversion efficiency. From this formula, the constant output current can be derived:

$$I_{OUTCC} = \frac{1}{2} \times L_P \times \left(\frac{0.396V \times 0.9}{R_{CS}} \right)^2 \times \left(\frac{\eta \times f_{SW}}{V_{OUTCV}} \right) \quad (2)$$

where f_{SW} is the switching frequency and V_{OUTCV} is the nominal secondary output voltage.

The constant current operation typically extends down to lower than 40% of nominal output voltage regulation.

Primary Inductance Compensation

The ACT334 integrates a built-in proprietary (patent-pending) primary inductance compensation circuit to maintain constant current regulation despite variations in transformer manufacturing. The compensated range is ±7%.

Primary Inductor Current Limit Compensation

The ACT334 integrates a primary inductor peak current limit compensation circuit to achieve constant input power over line and load ranges.

Protection

The ACT334 incorporates multiple protection functions including over-voltage, over-current and over-temperature.

Output Short Circuit Protection

When the secondary side output is short circuited, the ACT334 enters hiccup mode operation. In this condition, the VDD voltage drops below the V_{DDOFF} threshold and the auxiliary supply voltage collapses. This turns off the ACT334 and causes it to restart. This hiccup behavior continues until the short circuit is removed.

Output Over Voltage Protection

The ACT334 includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage for 4 consecutive switching cycles. The ACT334 enters hiccup mode when an output over voltage fault is detected.

Over Temperature Shutdown

The thermal shutdown circuitry detects the ACT334 die temperature. The typical over temperature threshold is 135°C with 20°C hysteresis. When the die temperature rises above this threshold the ACT334 is disabled until the die temperature falls by 20°C, at which point the ACT334 is re-enabled.

TYPICAL APPLICATION

Design Example

The design example below gives the procedure for a DCM flyback converter using the ACT334. Refer to Application Circuit in Figure 6, the design for a charger application starts with the following specification:

Input Voltage Range	85VAC - 265VAC, 50/60Hz
Output Power, P_O	5W
Output Voltage, V_{OUTCV}	5.0V
Full Load Current, I_{OUTFL}	1A
OCP Current, I_{OUTMAX}	1.3A
Transformer Efficiency, η_{xfm}	0.90
System Efficiency CC, η_{system}	0.72
System Efficiency CV, η	0.73

The operation for the circuit shown in Figure 6 is as follows: the rectifier bridge D1−D4 and the capacitor C1/C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and the startup resistor R7/R8. The primary power current path is formed by the transformer's primary winding, the NPN transistor, the ACT334 internal MOSFET and the current sense resistor R9. The network consisting of capacitor C4 and diode D6 provides a VDD supply voltage for ACT334 from the auxiliary winding of the transformer. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. The diode D8 and the capacitor C5 rectifies and filters the output voltage. The resistor divider consisting of R5 and R6 programs the output voltage.

The minimum and maximum DC input voltages can be calculated:

$$V_{INDCMIN} = \sqrt{2V_{ACMIN}^2 - \frac{2P_{OUT}\left(\frac{1}{2f_L} - t_C\right)}{\eta \times C_{IN}}} = \sqrt{2 \times 85^2 - \frac{2 \times 5\left(\frac{1}{2 \times 50} - 3.8ms\right)}{72\% \times 2 \times 6.8\mu F}} \approx 90V \quad (3)$$

$$V_{INDCMAX} = \sqrt{2} \times V_{ACMAX} = \sqrt{2} \times 265 = 375V \quad (4)$$

TYPICAL APPLICATION CONT'D

where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 2 × 6.8μF electrolytic capacitors based on the 3μF/W rule of thumb.

When the transistor is turned off, the voltage on the transistor's collector consists of the input voltage and the reflected voltage from the transformer's secondary winding. There is a ringing on the rising top edge of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by a RCD network if it is used. Design this clamped voltage as 50V below the breakdown of the NPN transistor. The flyback voltage has to be considered with selection of the maximum reverse voltage rating of secondary rectifier diode. If a 40V Schottky diode is used, then the flyback voltage can be calculated:

$$V_{RO} = \frac{V_{INDCMAX} \times (V_{OUTCV} + V_{DS})}{V_{DREV} - V_{OUTCV}} = \frac{375 \times (5 + 0.2)}{40 \times 0.8 - 5} = 73V \quad (5)$$

where V_{DS} is the Schottky diode forward voltage, V_{DREV} is the maximum reverse voltage rating of the diode and V_{OUTCV} is the output voltage.

The maximum duty cycle is set to be 45% at low line voltage $85V_{AC}$ and the circuit efficiency is estimated to be 73%. Then the full load input current is:

$$I_{IN} = \frac{V_{OUTCV} \times I_{OUTPL}}{V_{INDCMIN} \times \eta} = \frac{5 \times 1}{90 \times 72\%} = 75.6mA \quad (6)$$

The maximum input primary peak current at full load base on duty of 45%:

$$I_{PK} = \frac{2 \times I_{IN}}{D} = \frac{2 \times 75.6}{45\%} = 338\ mA \quad (7)$$

The primary inductance of the transformer:

$$L_P = \frac{V_{INDCMIN} \times D}{I_{PK} \times f_{SW}} = \frac{90 \times 45\%}{338mA \times 76kHz} \approx 1.6mH \quad (8)$$

ACT334 needs to work in DCM in all conditions, thus N_P/N_S should meet

$$\frac{L_P \times I_{PK}}{V_{INDCMIN}} + \frac{L_P \times I_{PK}}{(V_{OUTCV} + V_{DS}) \times \frac{N_P}{N_S}} < \frac{0.9}{f_{SW}} \Rightarrow \frac{N_P}{N_S} > 17.1 \quad (9)$$

The auxiliary to secondary turns ratio N_A/N_S:

$$\frac{N_A}{N_S} = \frac{V_{DD} + V_{DA} + V_R}{V_{OUTCV} + V_{DS} + V_{CORD}} = \frac{15 + 0.3 + 0.8}{5 + 0.20 + 0.402} = 2.87 \quad (10)$$

Where V_{DA} is diode forward voltage of the auxiliary side and V_R is the resister voltage.
An EFD15 transformer gapped core with an effective inductance A_{LE} of $82nH/T^2$ is selected. The number of turns of the primary winding is:

$$N_P = \sqrt{\frac{L_P}{A_{LE}}} = \sqrt{\frac{1.6mH}{82nH / T^2}} = 140 \quad (11)$$

The number of turns of secondary and auxiliary windings can be derived when Np/Ns=17.5:

$$N_S = \frac{N_S}{N_P} \times N_P = \frac{1}{17.5} \times 140 = 8 \quad (12)$$

$$N_A = \frac{N_A}{N_S} \times N_S = 2.87 \times 8 = 23 \quad (13)$$

The current sense resistance (R_{CS}) determines the current limit value based on the following equation:

$$R_{CS} = \frac{0.9 \times V_{CSLIM}}{\sqrt{\frac{(I_{OUTFL} + I_{OUTMAX}) \times V_{OUT}}{L_P \times f_{SW} \times \left(\frac{\eta_{system}}{\eta_{xfm}}\right)}}} = \frac{0.9 \times 0.396}{\sqrt{\frac{(1+1.3) \times 5}{1.6 \times 75 \times \left(\frac{0.72}{0.90}\right)}}} = 1R \quad (14)$$

The voltage feedback resistors are selected according to below equation:

$$R_{FB1} = \frac{N_A}{N_P} \times \frac{L_P}{R_{CS}} \times K = \frac{23}{140} \times \frac{1.6}{1} \times 229656 \approx 60.4k \quad (15)$$

Where K is IC constant and K = 229656.

$$R_{FB2} = \frac{V_{FB}}{(V_{OUTCV} + V_{DS}) \frac{N_A}{N_S} - V_{FB}} R_{FB1} = \frac{2.20}{(5 + 0.4) \times 2.87 - 2.20} \times 60.4 = 10.5k \quad (16)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUTCC} \times D}{f_{SW} \times \triangle V_{RIPPLE}} = \frac{1 \times 0.45}{75kHz \times 50mV} = 120\mu F \quad (17)$$

A 470μF electrolytic capacitor is used to keep the ripple small.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4), current sense resistor (R9) and feedback resistor (R5/R6) should be placed close to V_{DD}, CS and FB pins respectively. There are two main power path loops. One is formed by C1/C2, primary winding, NPN transistor and the ACT334. The other is the secondary winding, rectifier D8 and output capacitors (C5). Keep these loop areas as small as possible. Connect high current ground returns, the input capacitor ground lead, and the ACT334 G pin

TYPICAL APPLICATION CONT'D

to a single point (star ground configuration).

NPN Selection Guideline

NPN transistors with HFE of 20 to 30 are highly recommended in the design due to the start up time. If the HFE is too low the start up time becomes longer because of 30M start up resister.

V_{FB} Sampling Waveforms

ACT334 senses the output voltage information through the V_{FB} waveforms. Proper V_{FB} waveforms are required for IC to operate in a stable status. To avoid mis-sampling, 1.8μs blanking time is added to blank the ringing period due to the leakage inductance and the circuit parasitic capacitance.

Figure 2 is the recommended V_{FB} waveform to guarantee the correct sampling point so that the output information can be sent back into the IC to do the appropriate control.

V_{FB} waveforms of Figure 3, Figure 4, and Figure 5 violate the sampling design margin and are not recommended. Figure 3 has very long overshoot period. Figure 4, and Figure 5 have very long ringing period. The undesired waveforms cause the IC to operate in an unstable mode easily due to wrong feedback information.

Figure 2

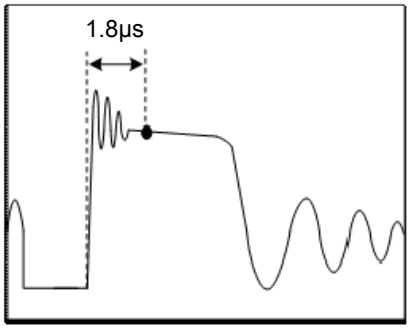


Figure 3

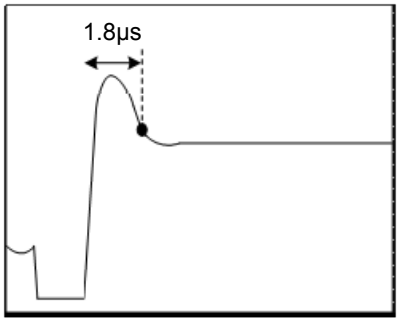


Figure 4

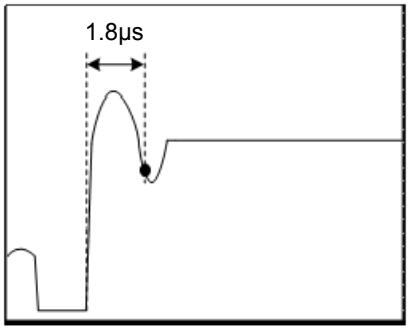


Figure 5

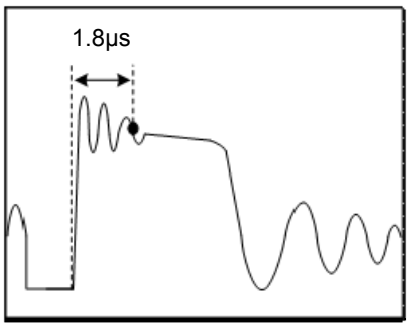


Figure 6:

Universal VAC Input, 5V/1A Output Charger

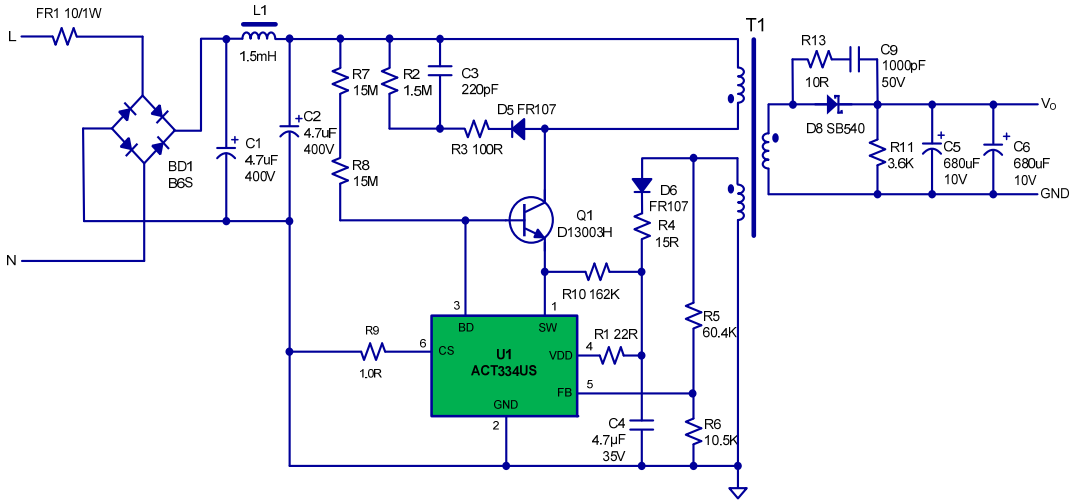


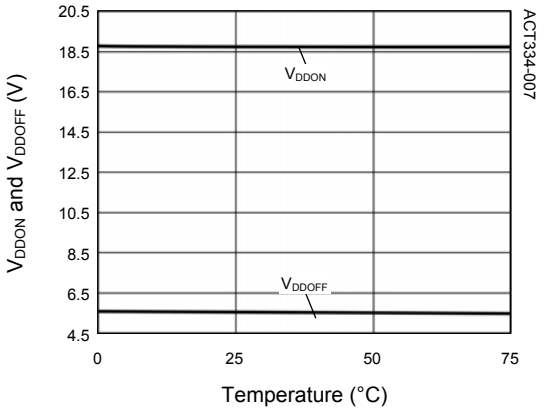
Table 1: ACT334 Bill of Materials

Item	Reference	Description	QTY
1	C1,C2	Capacitor, Electrolytic, 6.8μF/400V, 10x12mm（Low leakage current）	2
2	C3	Capacitor, Ceramic,220pF/500V,1206,SMD	1
3	C4	Capacitor, Ceramic,4.7μF/35V,1206,SMD	1
4	C5,C6	Capacitor, Electrolytic, 680μF/10V, 8x12mm	2
5	C9	Capacitor, Ceramic,1000pF/50V, 0805, SMD	1
6	D1-D4	Diode,Rectifier,1000V/1A,1N4007, DO-41	4
7	D5,D6	Diode,Ultra Fast, FR107,1000V/1.0A, DO-41	2
8	D8	Diode, schottky, 40V/5A, SB540, DO-15	1
9	L1	Axial Inductor, 1.5mH, 0410,Dip	1
10	Q1	Transistor, HFE 20-25, NPN,13003,TO-126	1
11	FR1	Wire Round Resistor,1W,10Ω, KNP, 5%	1
12	R2	Chip Resistor, 1.5mΩ, 1206, 5%	1
13	R3	Chip Resistor, 100Ω, 1206, 5%	1
14	R1	Chip Resistor, 22Ω, 0805, 5%	1
15	R4	Chip Resistor, 15Ω, 0805, 5%	1
16	R5	Chip Resistor, 60.4kΩ, 0805,1%	1
17	R6	Chip Resistor, 10.5kΩ, 0805, 1%	1
18	R7,R8	Chip Resistor, 15mΩ, 1206, 5%	2
19	R9	Chip Resistor, 1.0Ω, 1206,1%	1
20	R10	Chip Resistor, 162kΩ, 0805, 5%	1
21	R11	Chip Resistor, 3.6kΩ, 0805, 5%	1
22	R13	Chip Resistor, 10Ω, 0805, 5%	1
23	T1	Transformer, Lp=1.6mH, EFD15	1
24	U1	IC, ACT334US-T,SOT23-6	1

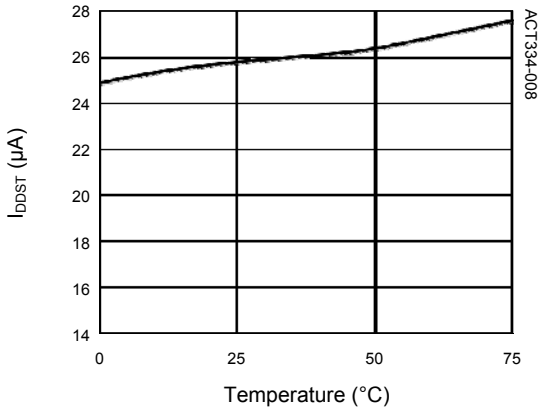
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(Circuit of Figure 6, unless otherwise specified.)

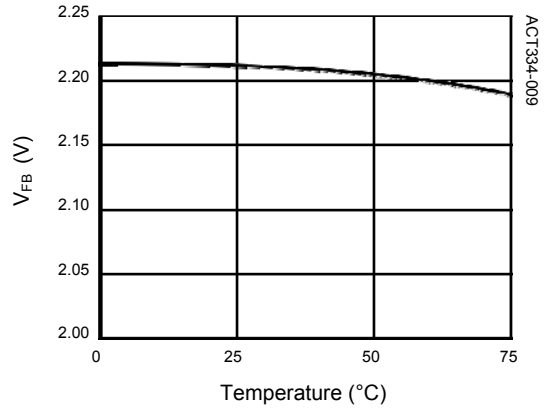
VDD ON/OFF Voltage vs. Temperature



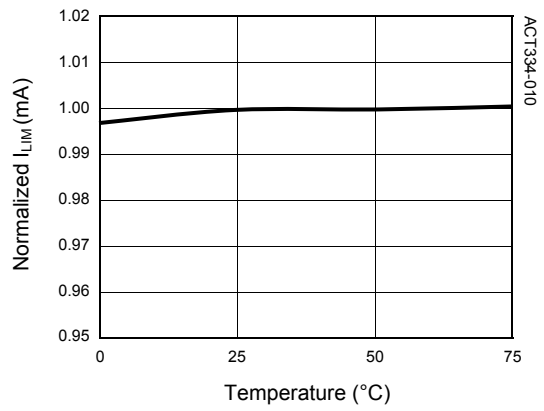
Start Up Supply Current vs. Temperature



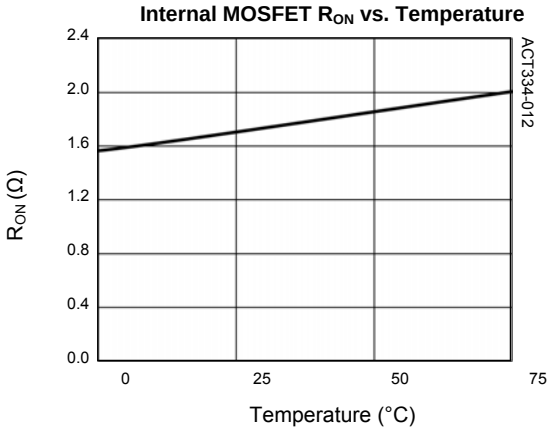
FB Voltage vs. Temperature



Normalized I_{LIM} vs. Temperature

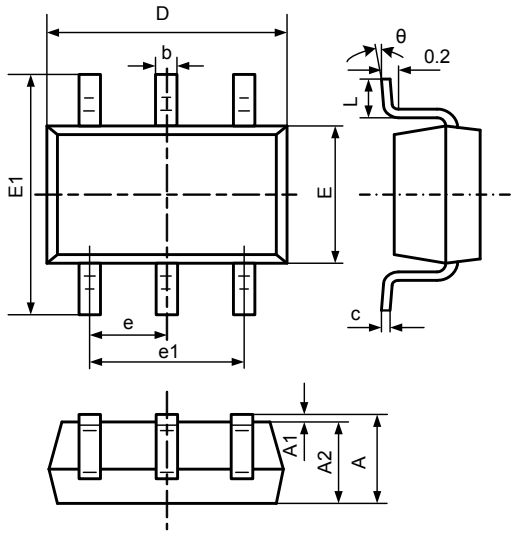


Internal MOSFET R_{ON} vs. Temperature



PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	-	1.450	-	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.900 BSC		0.114 BSC	
E	1.600 BSC		0.063 BSC	
E1	2.800 BSC		0.110 BSC	
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°